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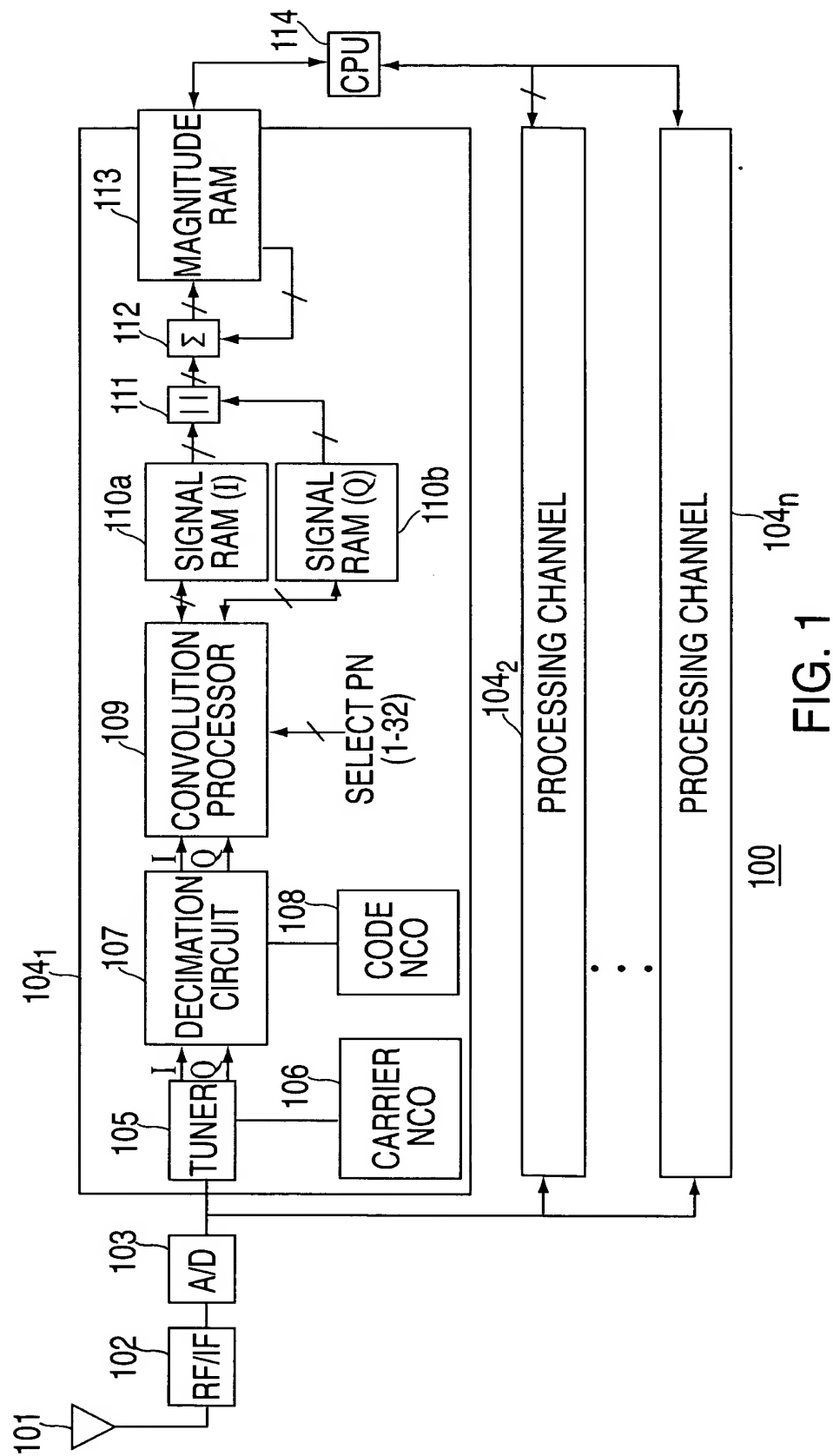


FIG. 1

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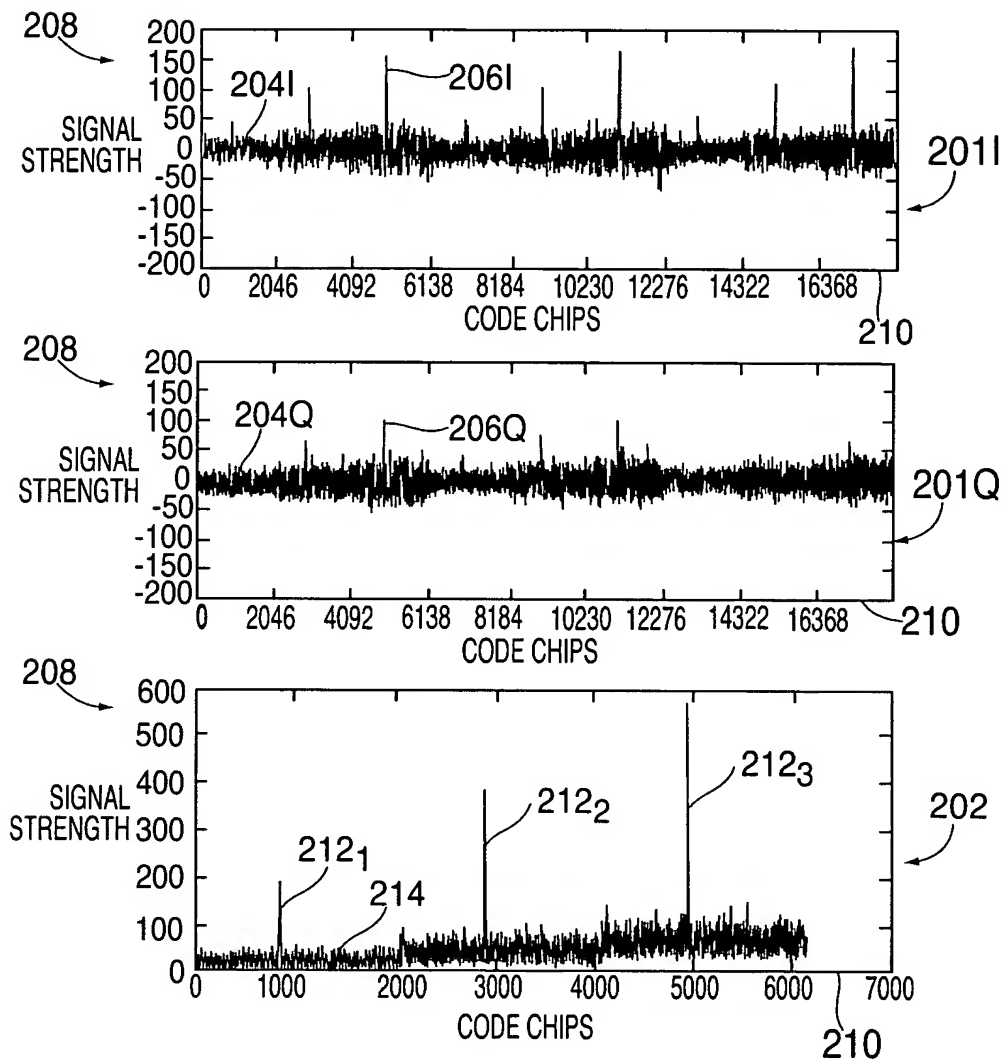


FIG. 2

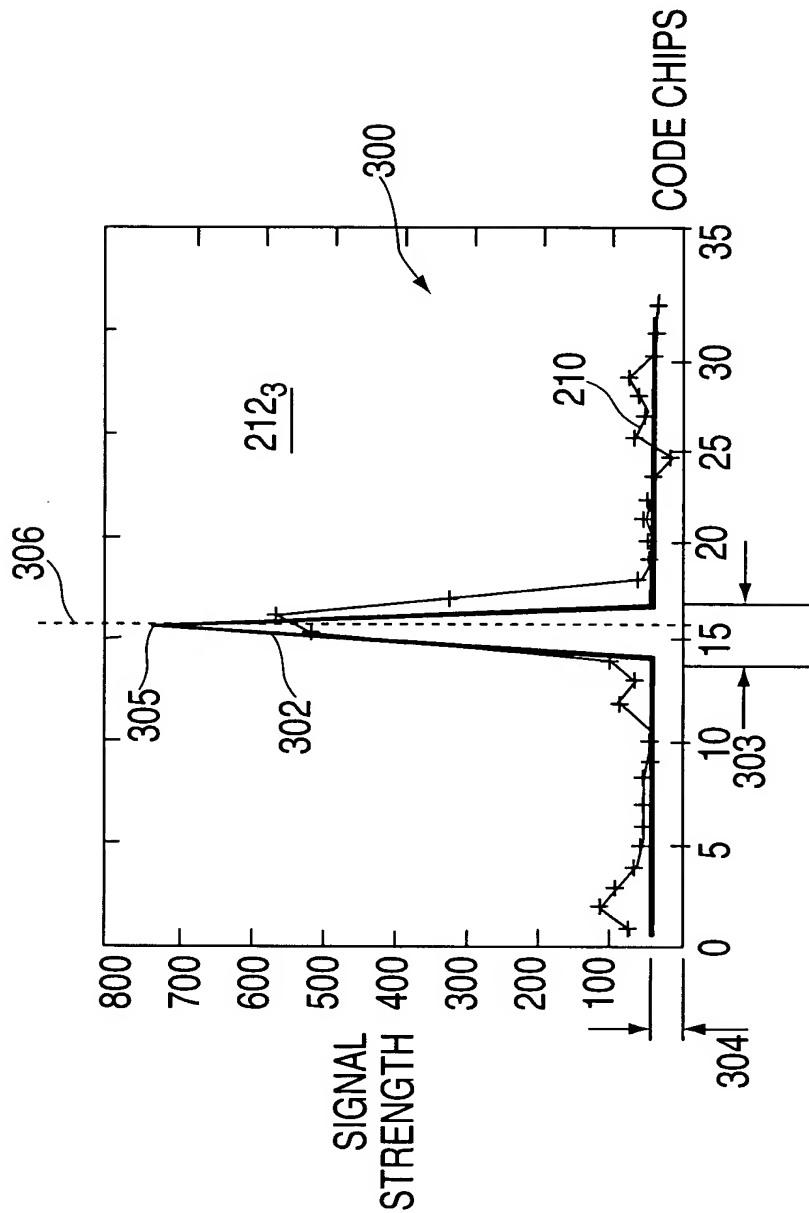


FIG. 3

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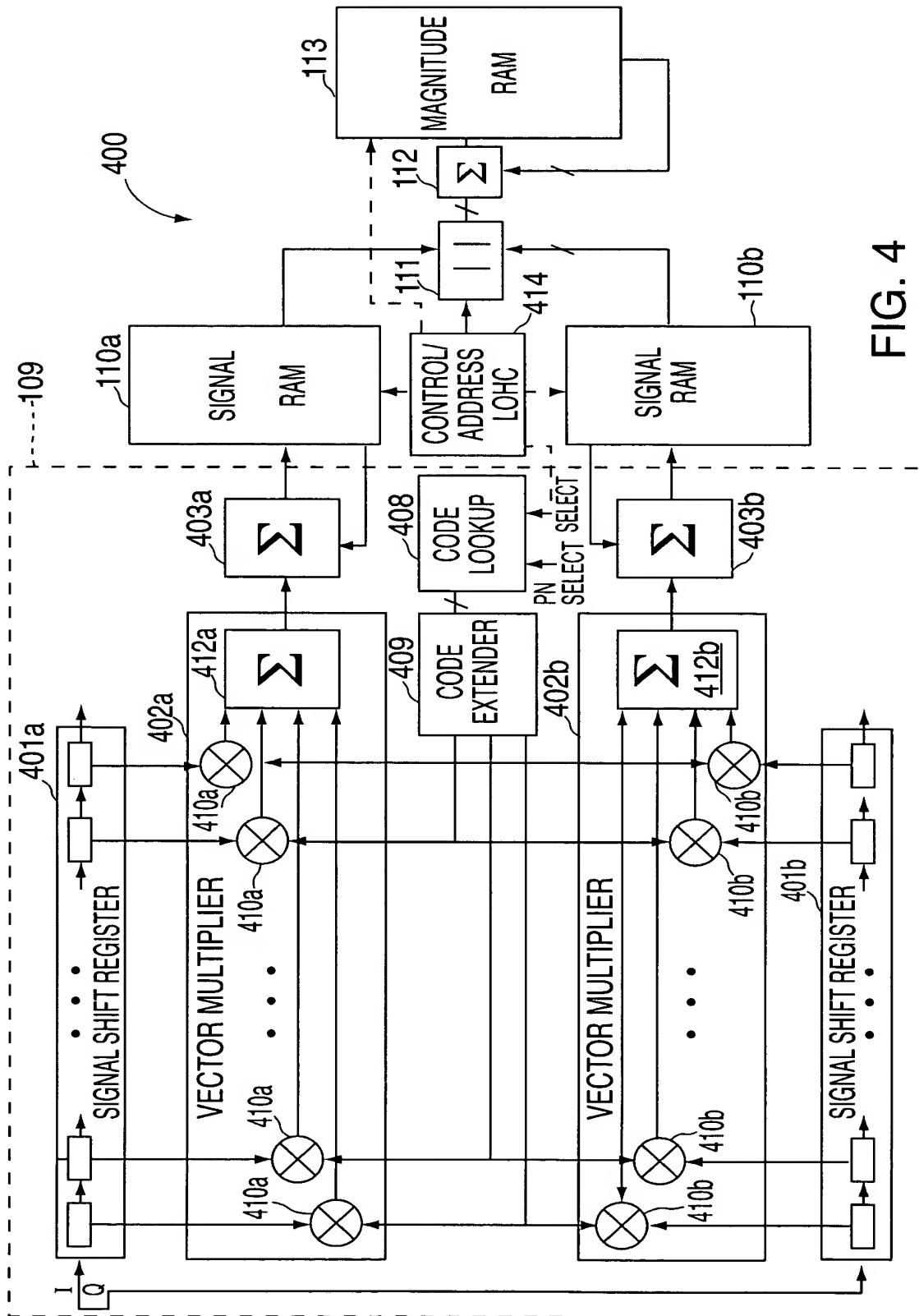


FIG. 4

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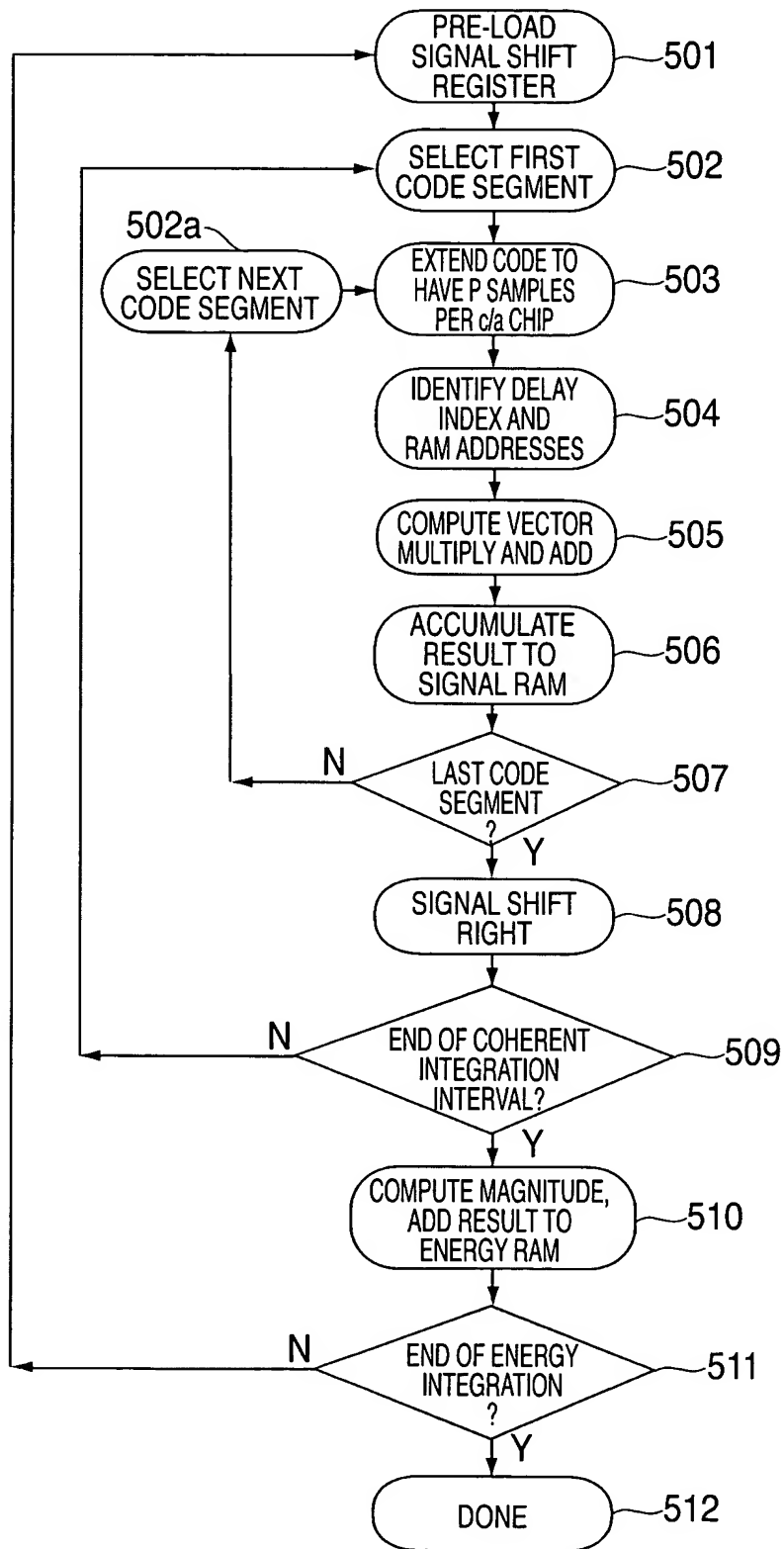


FIG. 5

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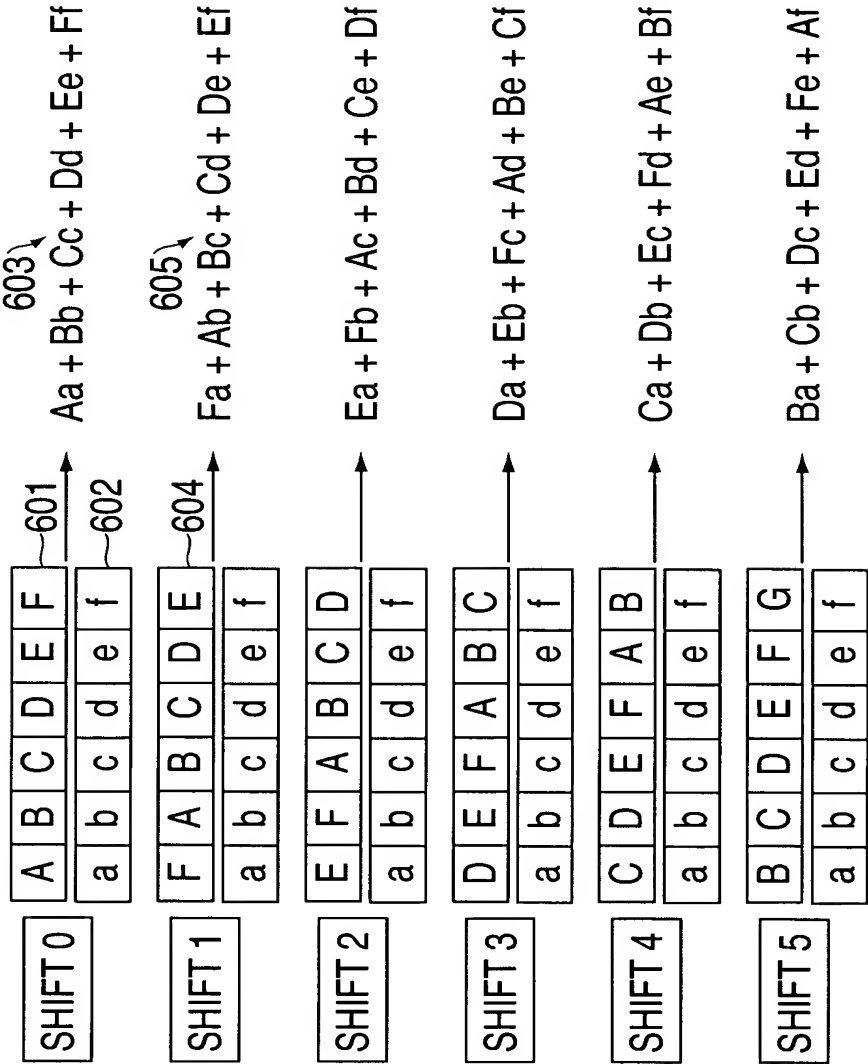
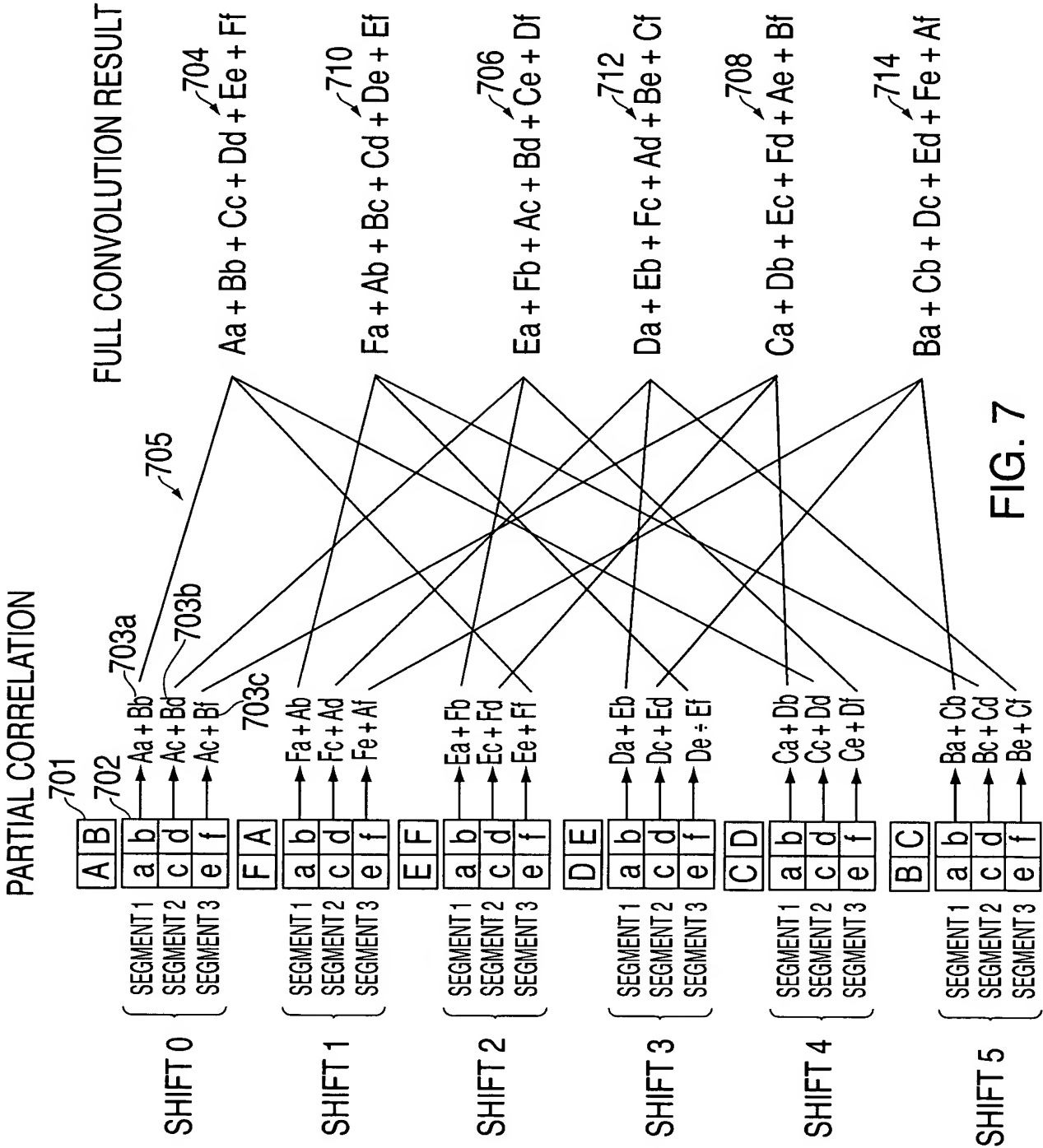


FIG. 6
(PRIOR ART)

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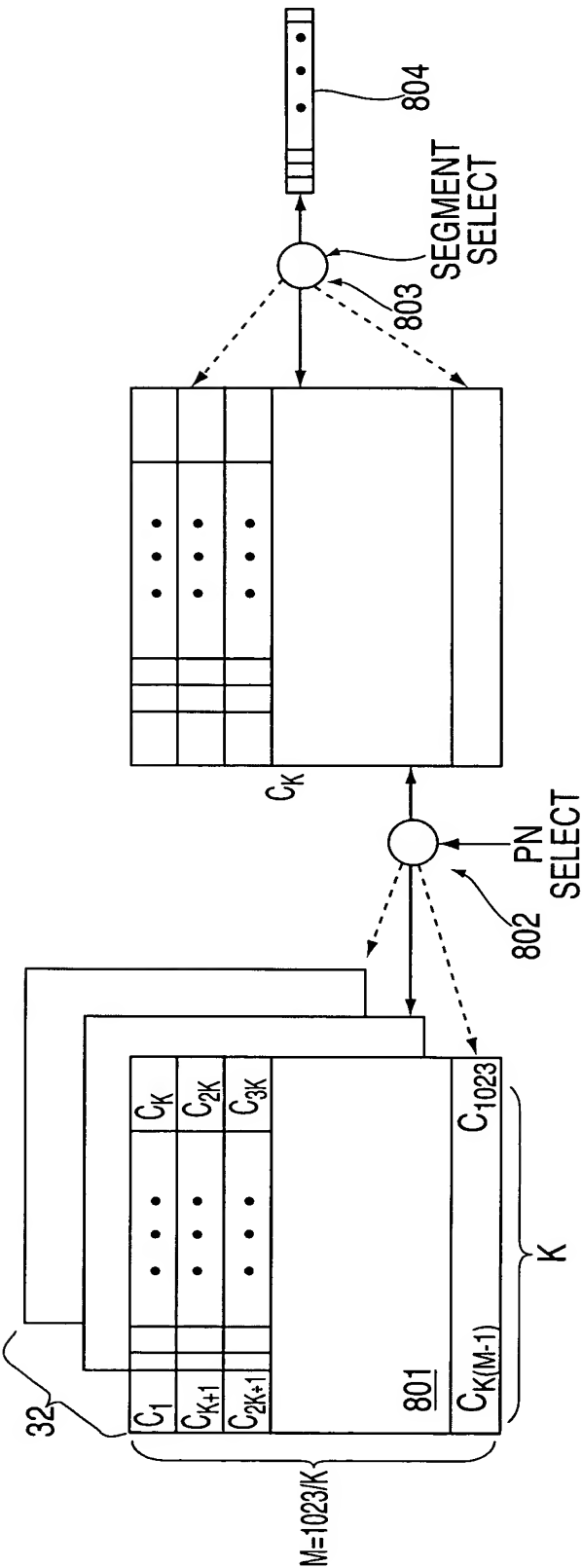
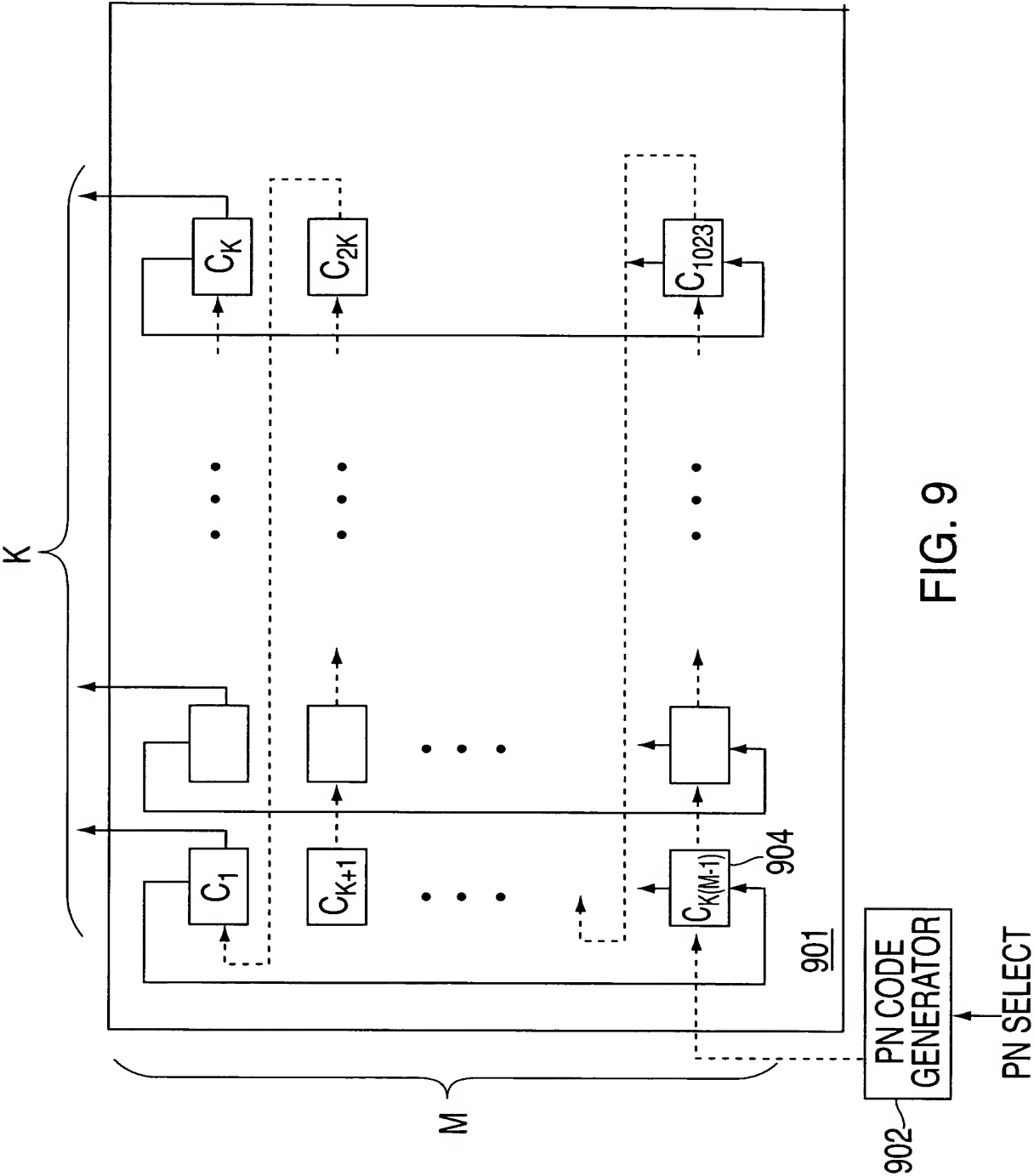


FIG. 8



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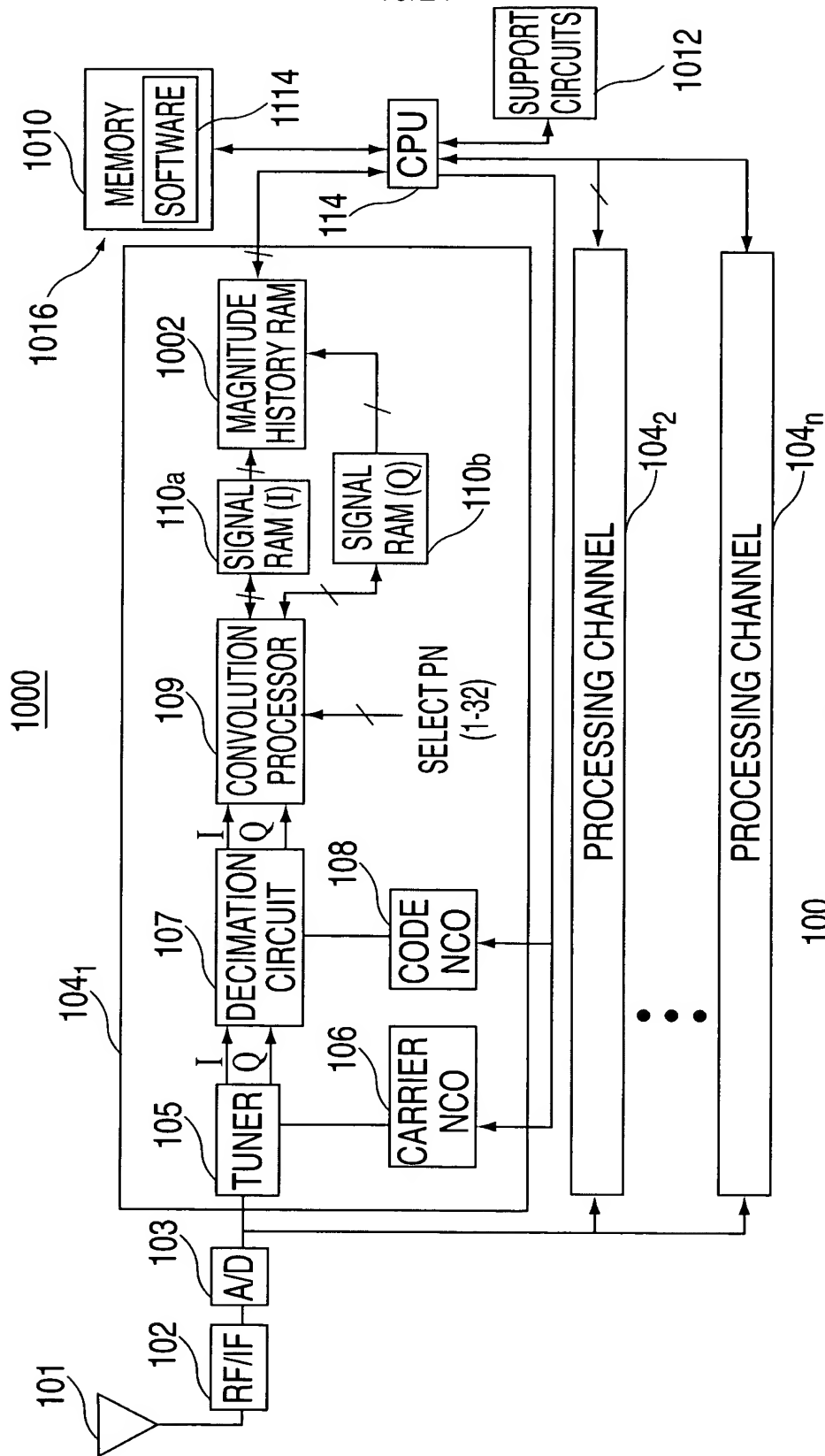


FIG. 10

		6 bits I	6 bits Q
RAM length	delay 1, epoch 1		
	delay 2, epoch 1		
	delay 3, epoch 1		
	delay 4, epoch 1		
	delay 1, epoch 2		
	delay 2, epoch 2		
	delay 3, epoch 2		
	delay 4, epoch 2		
	delay 1, epoch 3		
	delay 2, epoch 3		
	delay 3, epoch 3		
	delay 4, epoch 3		
	delay 1, epoch N		
	delay 2, epoch N		
	delay 3, epoch N		
	delay 4, epoch N		

FIG. 11

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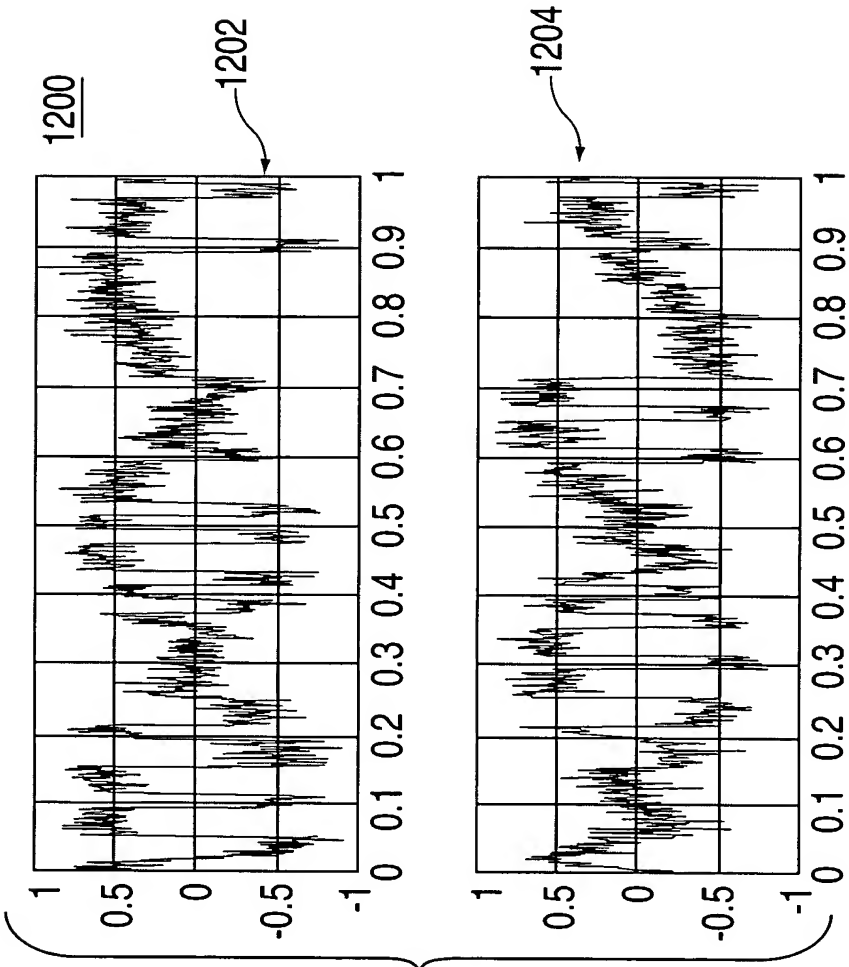
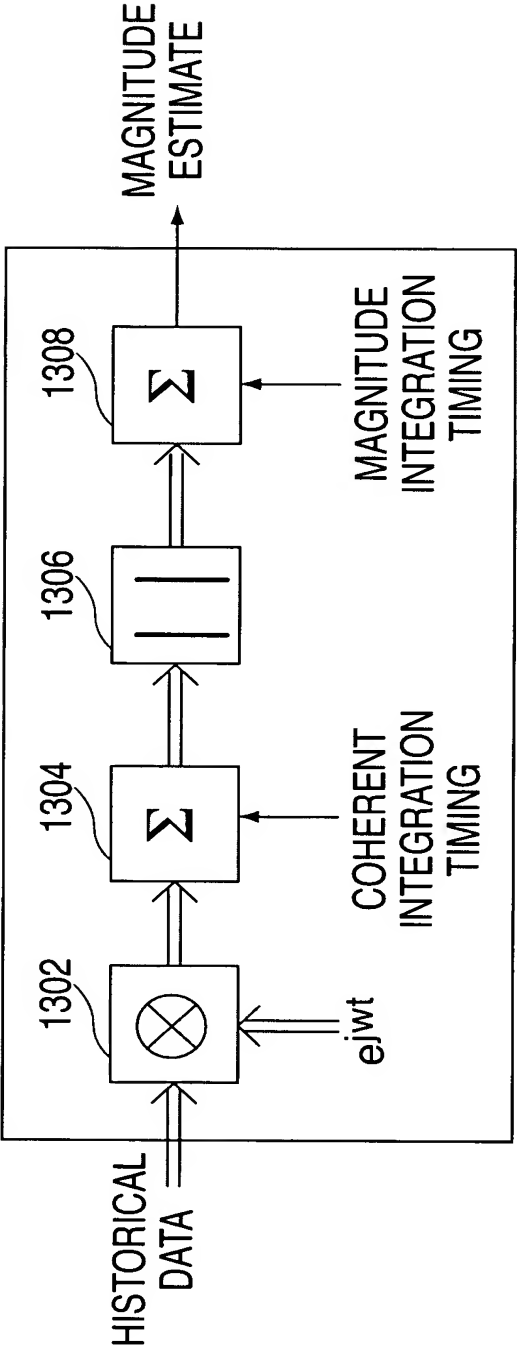


FIG. 12



1300

FIG. 13

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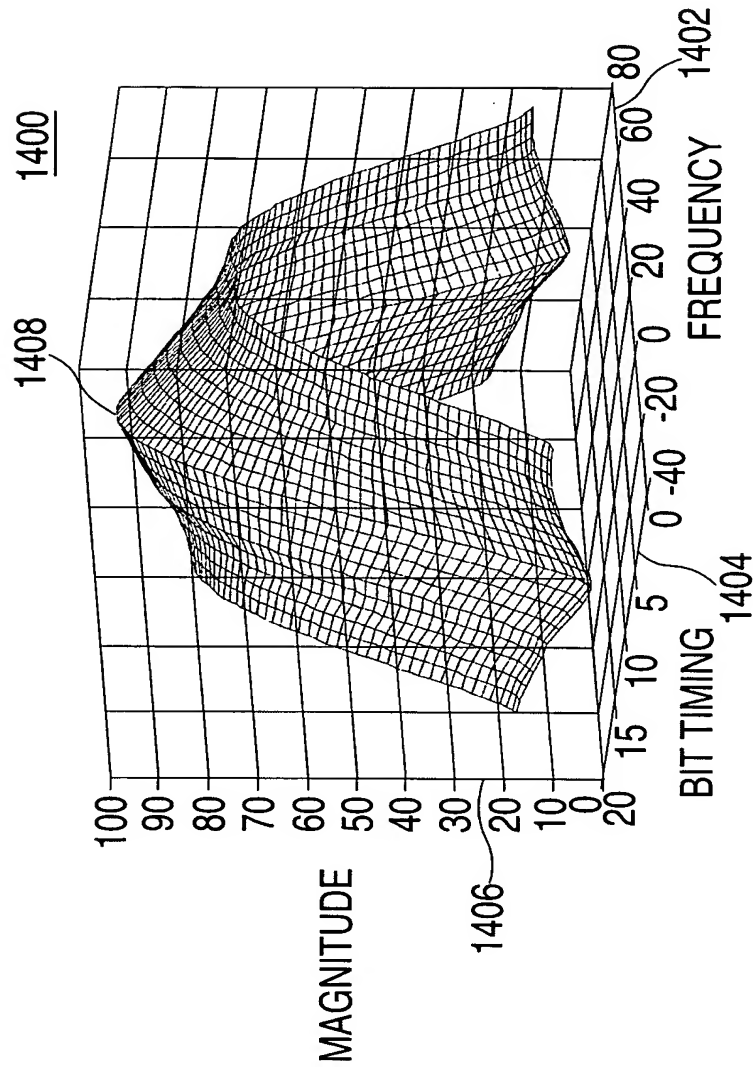


FIG. 14

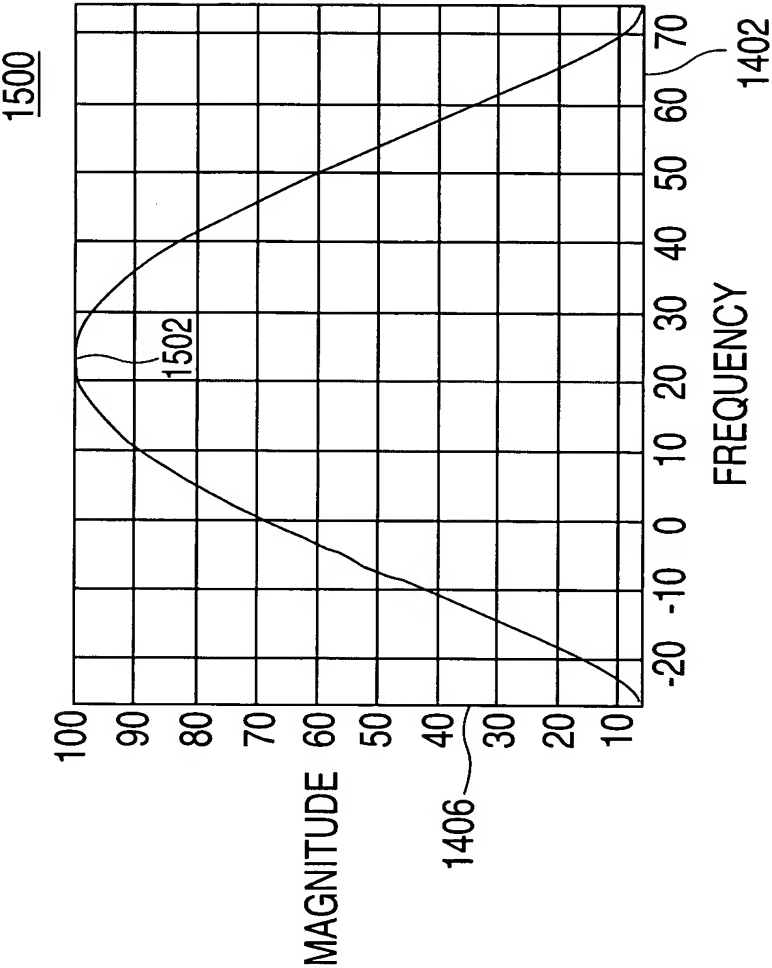


FIG. 15

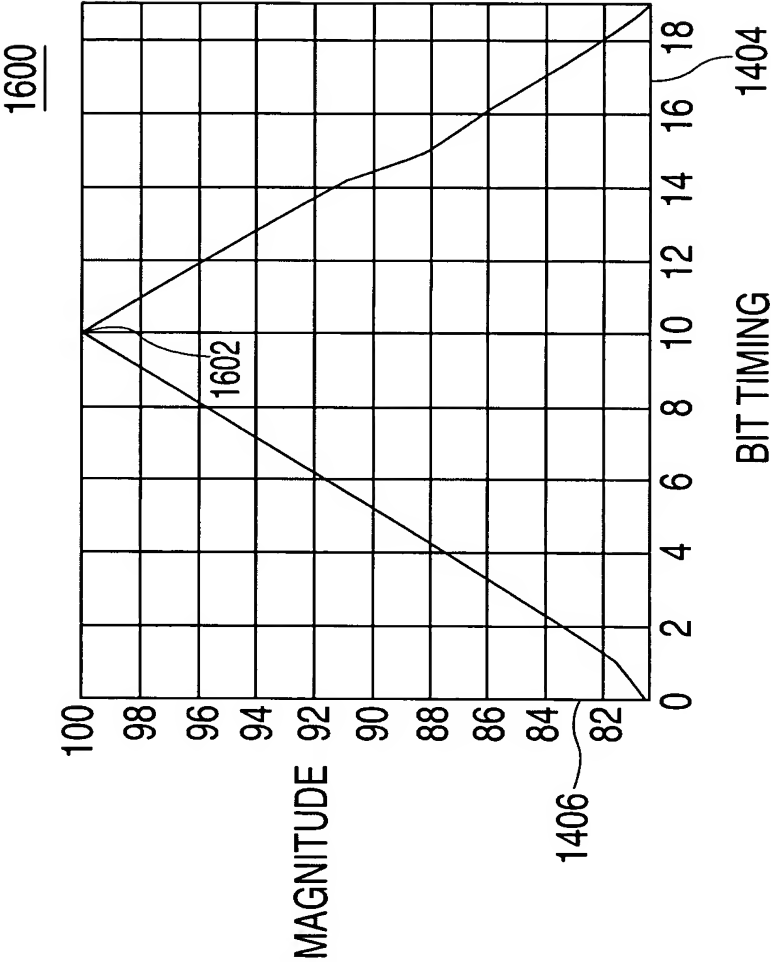


FIG. 16

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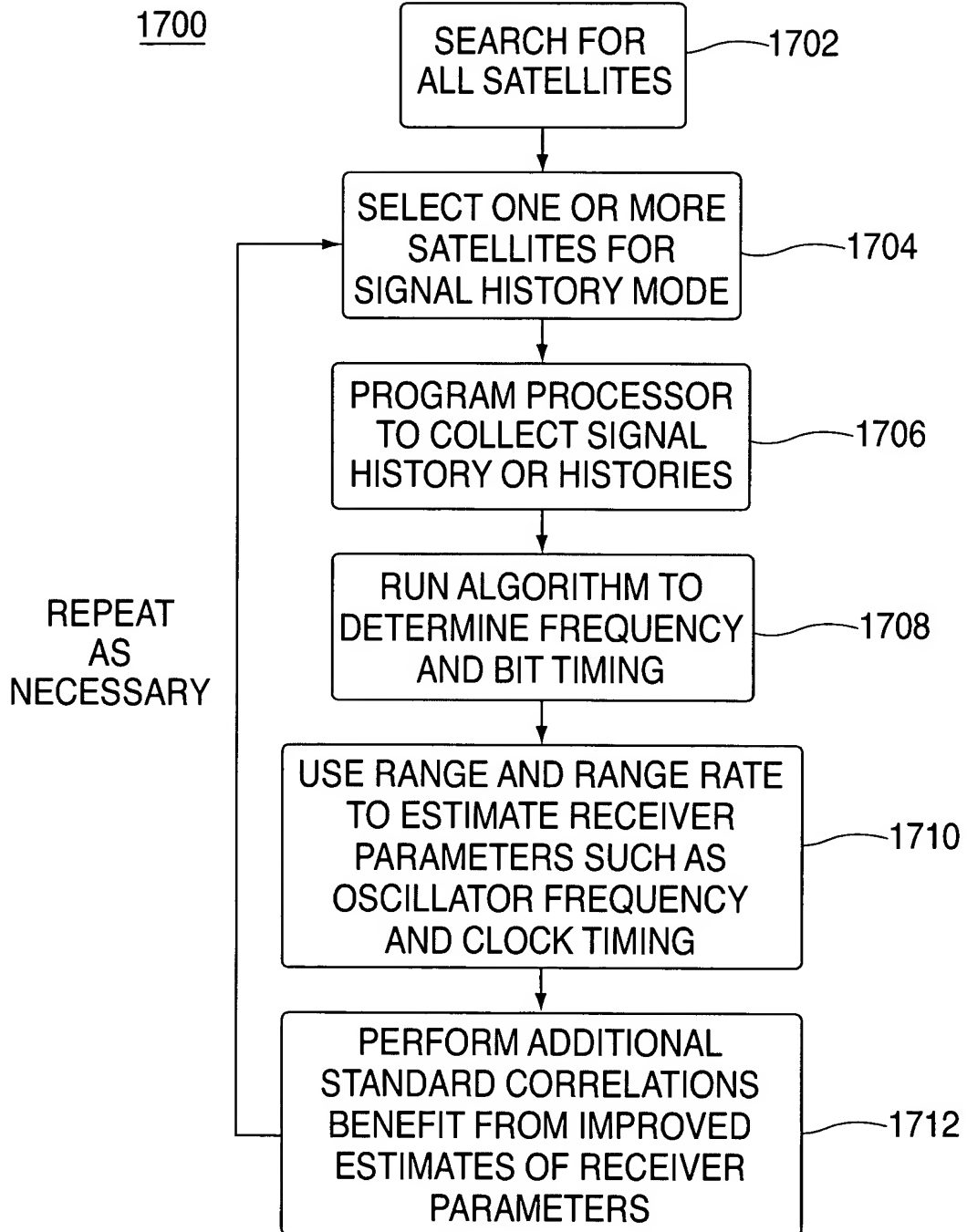


FIG. 17

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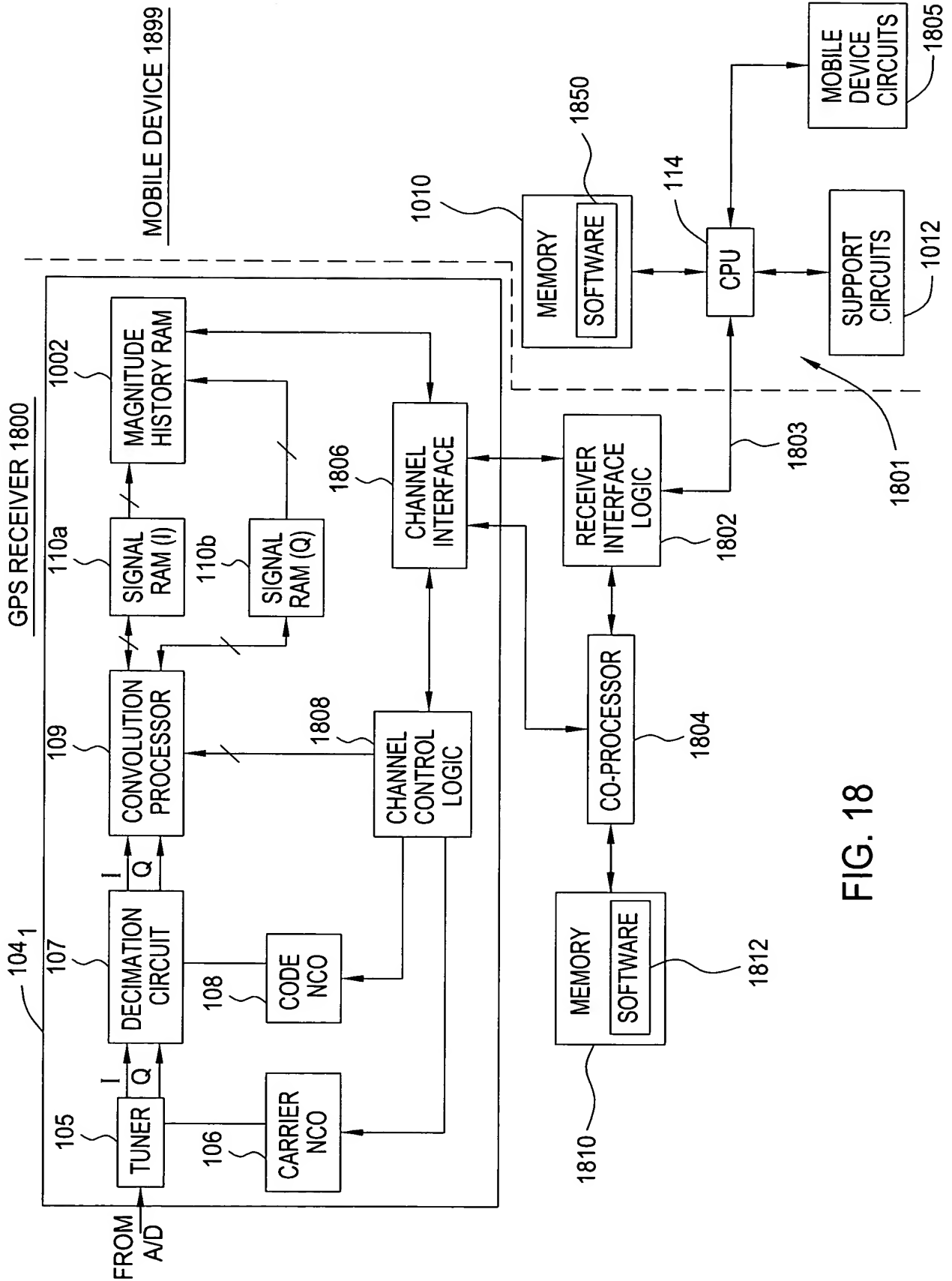


FIG. 18

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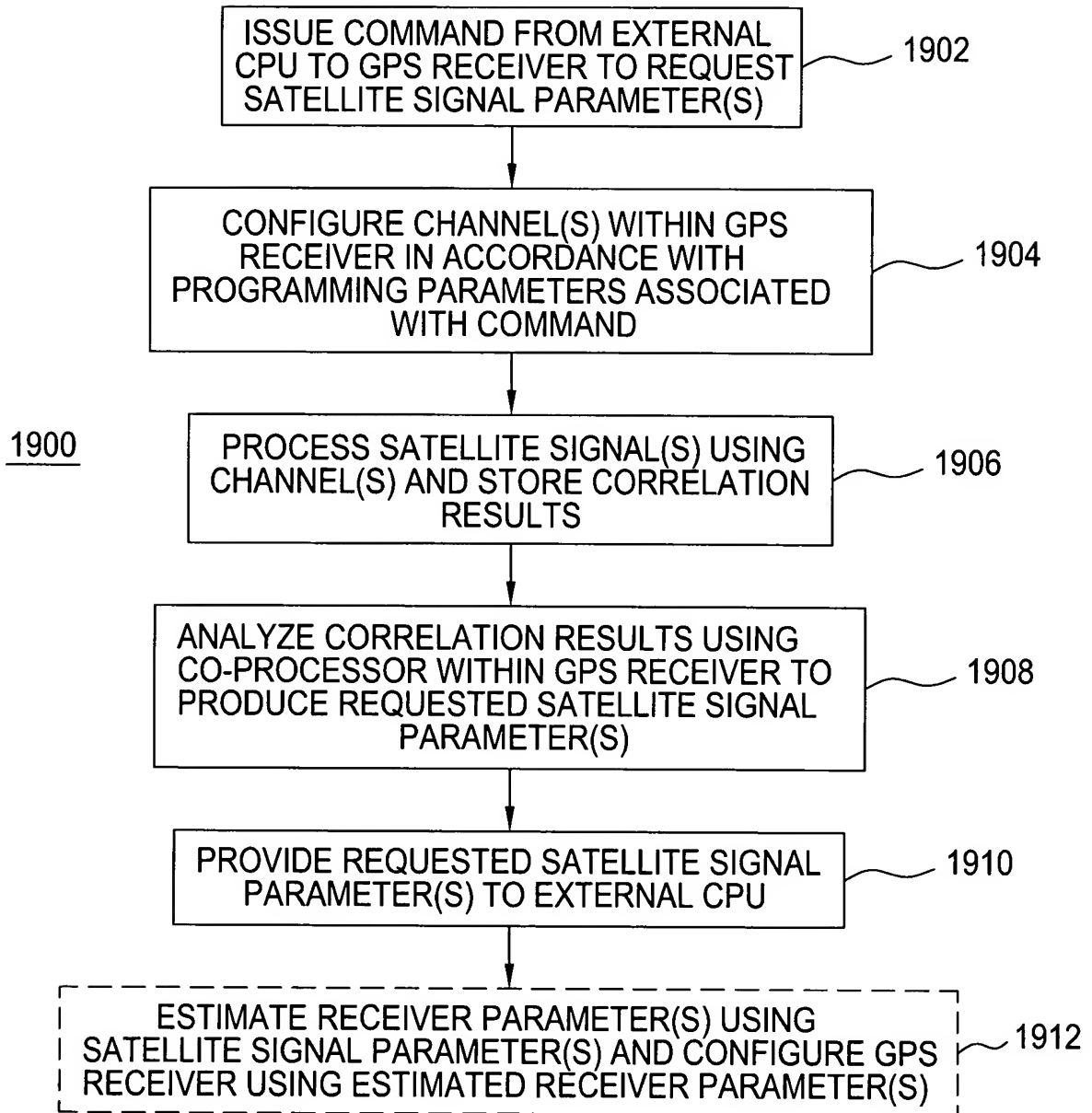


FIG. 19

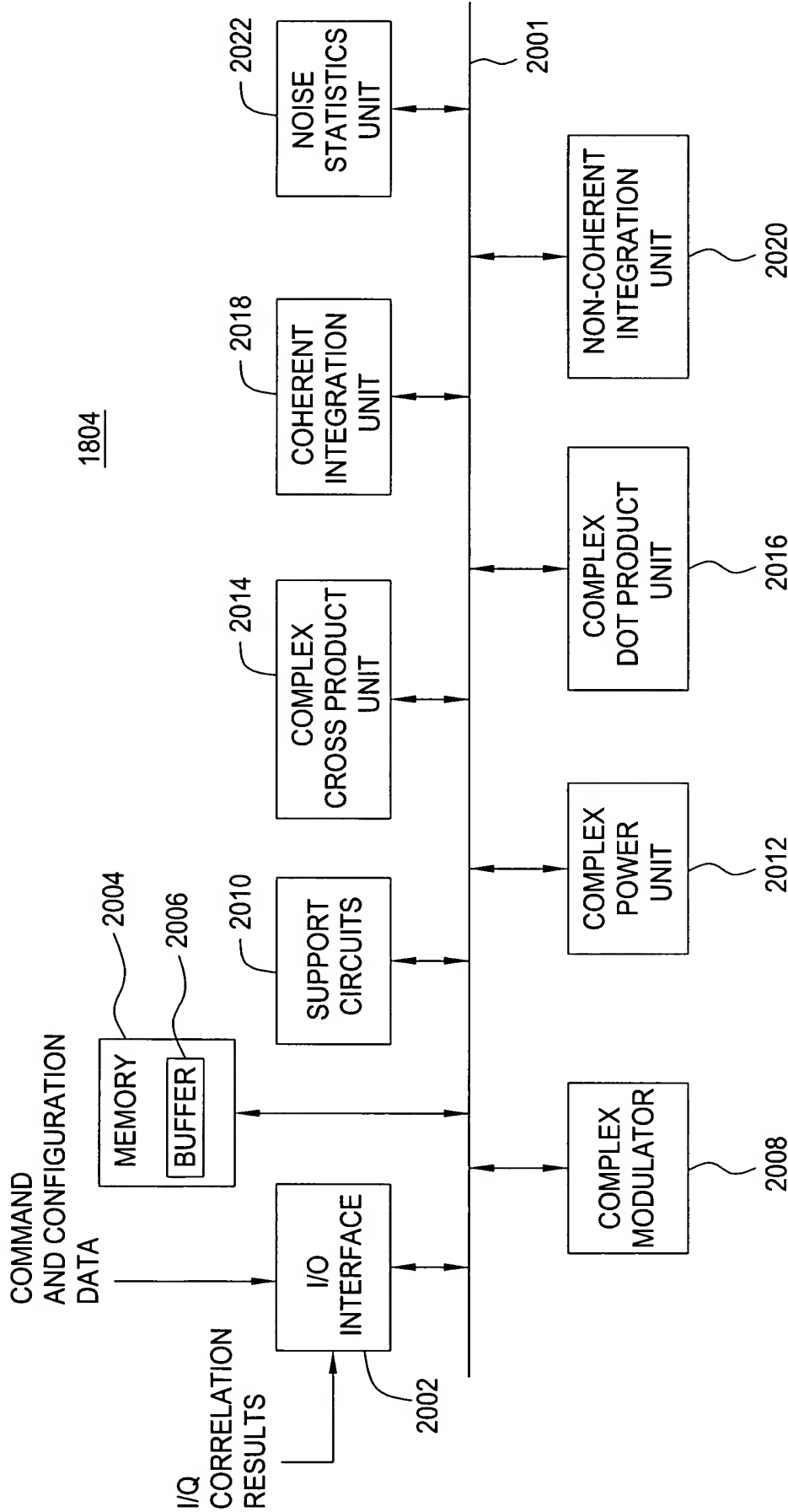


FIG. 20

